Simulation of Complex System Architecture

ABSTRACT OF THE DISCLOSURE

A method for simulating a chip is provided. The method initiates with defining a library of components for a processor. Then, the interconnections for a set of pipelined processors including the processor are defined. Next, a processor circuit is generated by combining the library of components and the interconnections for the set of pipelined processors. Then, a code representation of a model of the set of pipelined processors is generated. Next, the signals generated by the code representation are compared to the signals generated by the processor circuit. If the comparison of the signals is unacceptable, then the method includes identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit. A method for generating a netlist for a pipeline of processors, a method for debugging the processor circuit and computer code for simulating a chip circuit are also provided.